REMARKS

Claims 18-20 and 36-51 are pending in this application. By this Amendment, claims 18-19, 25-26 and 36 are amended, claims 1-17 and 21-35 are canceled, and claims 37-51 are added. New claims 40 and 46 generally correspond to canceled claims 7 and 13, respectively, and new claims 41-45 and 47-51 generally correspond to canceled claims 8-12 and 14-17 and 21, respectively. No new matter is added.

I. Allowable Subject Matter

Applicant appreciates the Office Action's indication that claims 18-20 contain allowable subject matter. Claims 18-19 have been rewritten in independent form, and claim 20 depends from claim 19. Thus, withdrawal of the objection to claims 18-20 is respectfully requested.

II. Claim Rejections Under 35 U.S.C. §102(e)

A. Yamagishi

The Office Action rejects claims 1-17, 21 and 36 under 35 U.S.C. §102(e) over U.S. Patent No. 6,501,466 (Yamagishi). This rejection is respectfully traversed.

Claims 1-17 and 21 are canceled. Claim 40 generally corresponds to canceled claim 7 and claim 46 generally corresponds to canceled independent claim 13. These rejections will be discussed with respect to new claims 40 and 46.

Claim 40 recites, in part, a "method of driving an electronic device including a plurality of first signal lines, a plurality of second signal lines, a plurality of *power-supply lines that intersect the plurality of second signal lines*, and a plurality of unit circuits . . ." (emphasis added).

Claim 46 recites, in part, a "method of driving an electro-optical device including a plurality of first scanning lines, a plurality of second scanning lines, a plurality of data lines, a

plurality of *power-supply lines that intersect the plurality of data lines*, and a plurality of unit circuits . . ." (emphasis added).

Both Claims 40 and 46 also recite, in part, "the first gate being electrically connected to one power-supply line of the plurality of power-supply lines during at least a part of the second period."

Yamagishi discloses an active matrix type display apparatus and drive circuit thereof. The drive circuit includes a data line DATA and two scan lines, SCAN-A and SCAN-B. A capacitor C is connected to a potential Vdd (power potential)(allegedly corresponding to the claimed power-supply lines). Fig. 1 of Yamagishi clearly shows that SCAN-A, SCAN-B, and DATA do not intersect Vdd. Therefore, Yamagishi does not teach or suggest at least "a plurality of power-supply lines that intersect the plurality of second signal lines" or "a plurality of power-supply lines that intersect the plurality of data lines." Further, Yamagishi does not teach or suggest "the first gate being electrically connected to one power-supply line of the plurality of power-supply lines during at least a part of the second period." Thus, for at least these reasons claims 40 and 46 are not anticipated by Yamagishi.

Further, claims 36, 41-45 and 47-51, which variously depend from claims 40 and 46, are not anticipated by Yamagishi at least based on their dependence on allowable base claims, as well as for additional features they recite.

B. Hiroshi

The Office Action rejects claims 1, 7 and 13 under 35 U.S.C. §102(e) over JP 2003-216100. This rejection is respectfully traversed, as if applied to new claims 40 and 46.

Hiroshi, like Yamagishi, fails to teach or suggest at least a "plurality of power-supply lines that intersect the plurality of second signal lines," a "plurality of power-supply lines that intersect the plurality of data lines" and "the first gate being electrically connected to one

power-supply line of the plurality of power-supply lines during at least a part of the second period." Thus, for at least these reasons, claims 36 and 40-51 are not anticipated by Hiroshi.

III. New Claims 37-39

New Claim 37 recites, in part, "the third transistor included in each of the plurality of unit circuits being in an off-state during a fourth period from a first time when the setting of the conduction state of the first transistor included in the first set of unit circuits is completed to a second time when the turning on the second transistor included in the second set of unit circuits commences." This feature is neither taught nor suggested by the cited prior art references.

IV. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 18-20 and 36-51 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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